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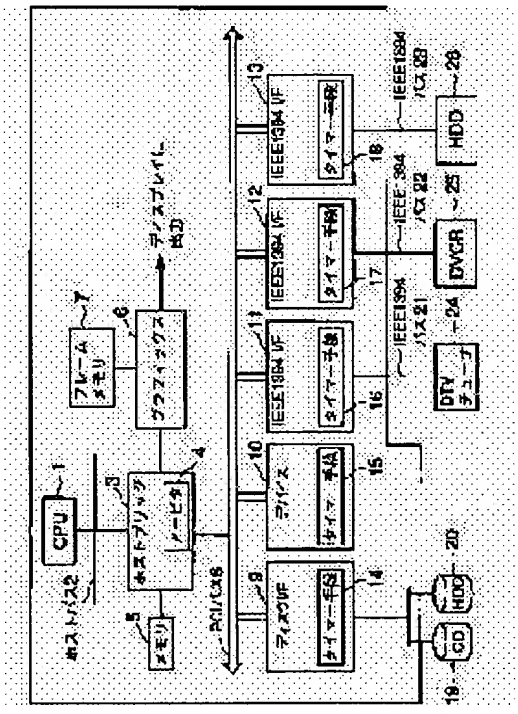
(54) COMPUTER AND PROGRAM RECORDING MEDIUM

(57)Abstract:

PROBLEM TO BE SOLVED: To solve a problem that synchronizing data are not normally processed when a large amount of data are transmitted in a computer.

SOLUTION: The computer is provided with a PCI bus 8, synchronizing devices 11-13 for transmitting synchronizing data which require the guarantee of a transmission band through the PCI bus 8, synchronizing devices 9 and 10 for transmitting asynchronous data which do not require the guarantee of the transmission band through the PCI bus 8, an arbiter 4 for giving a permission to use the bus fairly or by giving preference to the synchronizing devices with respect to a request for using the bus 8 and a CPU for at least processing data to be transmitted through the PCI bus 8 or controlling the synchronizing devices and the synchronizing devices.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the computer and program documentation medium which can process real-time data to be guaranteed [of a transmission band] at the time of transmission.
[0002]
[Description of the Prior Art] The computer which can process real-time data to be guaranteed [of a transmission band] at the time of the conventional transmission is explained using drawing 16 .
[0003] In drawing 16 , a computer consists of CPU1, the host bus 2, a host bridge 100, memory 5, graphics 6, a frame memory 7, PCI bus 8, disk I/F9, a device 10, and IEEE1394I/F 101-103.
[0004] Moreover, CD19 and HDD20 are connected to disk I/F9. The DTV tuner 24 is connected to IEEE1394I/F101 through the IEEE1394 bus 21. DVCR25 is connected to IEEE1394I/F102 through the IEEE1394 bus 22. HDD26 is connected to IEEE1394I/F103 through the IEEE1394 bus 23.
[0005] CPUs1 are data processing and a means to perform an operation. The host bus 2 is a processor bus by which CPU1 and memory 5 are made as for data transmission to an epilogue and ultra high-speed. A host bridge 100 is a control chip which controls delivery of the data between CPU1, memory 5, and PCI bus 8. Memory 5 is SDRAM (synchronous dynamic access memory) which records data. Graphics 6 are means to be connected with a host bridge 100 by AGP which can carry out data transmission to a high speed, and to draw graphics at a high speed by it. A frame memory 7 is a means to hold the image data of a display screen as bit map data.
[0006] PCI bus 8 is a bus in the interior of the computer which two or more devices share. Disk I/F9 is an interface of SCSI conformity which connects CD19 and HDD20 with PCI bus 8. A device 10 is equipment connected to PCI bus 8. IEEE1394I/F 101-103 is the interface of the IEEE1394 conformity which ties PCI bus 8 and the IEEE1394 buses 21-23, respectively. The IEEE1394 buses 21-22 are IEEE1394 buses of another network which have the bus ID according to individual, respectively.
[0007] CD19 is equipment which reads the data of CD-ROM and is connected to disk I/F9. HDD20 is a hard disk which records data by random access or reads them, and is equipment connected to disk I/F9.
[0008] It connects with the IEEE1394 bus 21 and the DTV tuner 24 is a tuner which receives the digital approaches, such as CS broadcasting. It connects with the IEEE1394 bus 22 and DVCR25 is a digital video cassette recorder which performs record and playback of AV data. HDD26 is a hard disk which is connected to the IEEE1394 bus 22 and performs record and playback of AV data.
[0009] Moreover, IEEE1394 is the specification of a bus that real-time data to be guaranteed [of a transmission band] can be sent. The thing of the IEEE1394 interfaces 101-103 which can transmit synchronous data, and a call and synchronous data for the thing of real-time data below is called a synchronous device. Moreover, the thing of a device which transmits the data which do not need the guarantee of transmission bands, such as disk I/F9 and a device 10, is made to call an asynchronous data the thing of an asynchronous device and the data which do not need the guarantee of a call and a transmission band.
[0010] Next, actuation of such a conventional computer is explained.

[0011] First, the DTV tuner 24 explains the actuation in the case of receiving CS broadcasting.
[0012] AV data have been carried and sent to the broadcast wave from the broadcasting station of CS broadcasting using the transport packet of an MPEG 2 transport stream.
[0013] First, the DTV tuner 24 requires the transmission band for transmitting AV data to the device which is an isochronous resource manager among the equipment connected to the IEEE1394 bus 21. An isochronous resource manager secures a transmission band for the DTV tuner 24 to transmit AV data, and gives a channel number.
[0014] The DTV tuner 24 receives this broadcast wave, and gets over. And the DTV tuner 24 sends out AV data to which it restored to the IEEE1394 bus 21 as an isochronous packet one by one using the channel number to which it was given by the isochronous resource manager.
[0015] IEEE1394I/F101 requires a bus royalty of the arbiter in a host bridge 100. An arbiter performs a bus arbitration and grants a bus royalty to IEEE1394I/F101. Thus, IEEE1394I/F101 becomes the initiator of PCI bus 8.
[0016] Next, IEEE1394I/F101 discriminates the isochronous packet which the DTV tuner 24 sent from a channel number, and receives. And once storing received AV data in a buffer, the address of the host bridge 100 which is a target is specified, and it sends out to PCI bus 8.
[0017] A host bridge 100 receives AV data sent from IEEE1394I/F101, and stores them in memory 5 as a transport packet of an MPEG 2 transport stream. CPU1 separates AV data stored in memory 5, and makes them an elementary stream. AV data changed into the elementary stream are sent to graphics 6 through a host bridge 100.
[0018] GURAFUKKUSU 6 carries out AV decoding of the sent AV data of an elementary stream. And the image data obtained as a result of carrying out AV decoding is written in a frame memory. Moreover, graphics 6 read the image data stored in the frame memory 7, and change it into an RGB code. This RGB code is sent to a display.
[0019] Finally, a display displays the image received with the DTV tuner 24.
[0020] Thus, the conventional computer processes data to be guaranteed [of a transmission band].
[0021] Next, the actuation whose computer 1 executes the application program stored in HDD20 is explained.
[0022] Disk I/F9 requires a bus royalty of the arbiter in the interior of a host bridge 100. An arbiter performs a bus arbitration and grants a bus royalty to disk I/F9. Thus, disk I/F9 becomes the initiator of PCI bus 8.
[0023] Next, disk I/F9 reads the application program stored in HDD20, and sends it to a host bridge 100. A host bridge 100 stores the received application program in memory 5.
[0024] CPU1 executes the instruction of the address with which the program counter of the application program stored in memory 5 expresses. The result to which CPU1 executed the instruction of an application program is stored in memory 5. And the data outputted to a display among the result are sent to GURAFUKKUSU 6 through a host bridge 100.
[0025] Graphics 6 carry out scanning conversion of the graphic data, such as a vector font, a circle, and a straight line, change them into image data, and are written in a frame memory 7. Moreover, graphics 6 read the image data stored in the frame memory 7, and change it into an RGB code. This RGB code is sent to a display.
[0026] Finally, a display displays the activation result of an application program.
[0027] Thus, a computer executes a program.
[0028]
[Problem(s) to be Solved by the Invention] By conventional computer mentioned above, although two actuation is explained separately, these two actuation may be performed by coincidence. Moreover, generally IEEE1394I/F101 may transmit synchronous data to that disk I/F9, a device 10, etc. transmit an asynchronous data and coincidence. That is, it may be performed to coincidence that two or more asynchronous devices' transmitting an asynchronous data and a synchronous device transmit synchronous data.
[0029] In such a case, the rate to which each device transmits data becomes large. That is, if the rate

which can be transmitted is full of the internal bus of the computer which two or more devices, such as PCI bus 8, share and it will be in the condition of transmitting data, although each device transmits data to the internal bus of a computer, a waiting state will arise. And when a synchronous device transmits synchronous data, the transmission band which should be guaranteed cannot be secured but the technical problem of it becoming impossible to transmit data normally occurs.

[0030] Moreover, when two or more devices perform access to memory to coincidence, the latency time arises in that by which a synchronous device writes synchronous data in memory (or it reads from memory), and the technical problem that data can be normally written in memory (or it reads from memory) occurs.

[0031] Moreover, since processing of other tasks is performed to coincidence when OS can perform a multitask operation, a waiting state arises at processing of synchronous data, and the technical problem that the case where it does not do at the transmission rate of the synchronous data which should be guaranteed arises occurs.

[0032] Moreover, as for the clock supplied to the cycle-time register of the IEEE1394 bus 21, and the clock supplied to the cycle-time register of the IEEE1394 bus 22, the frequency does not synchronize. Moreover, the cycle-time register of the IEEE1394 bus 21 and the cycle-time register of the IEEE1394 bus 22 mince another time of day. Moreover, when it goes via PCI bus 8, delay arises as compared with the case where it does not go via PCI bus 8. Therefore, AV data received with the DTV tuner 24 are unrecordable on DVCR25 via PCI bus 8. That is, the technical problem that synchronous data cannot be sent is in the IEEE1394 interface connected to another IEEE1394 bus from the IEEE1394 interface connected to one IEEE1394 bus via the internal bus of the computer which two or more devices, such as a PCI bus, share.

[0033] If a lot of data are transmitted to the internal bus of a computer which two or more devices share, this invention will aim at offering the computer which can transmit synchronous data normally, even if a lot of data are transmitted to the internal bus of a computer with which two or more devices share synchronous data in consideration of the technical problem that it cannot transmit normally.

[0034] Moreover, when, as for this invention, two or more devices perform access to memory to coincidence, The latency time arises in that by which a synchronous device writes synchronous data in memory (or it reads from memory). Even if two or more devices perform access to memory to coincidence in consideration of the technical problem that synchronous data can be normally written in memory (or it reads from memory) A synchronous device aims at offering the computer which can write synchronous data in memory (or it reads from memory).

[0035] Moreover, since processing of other tasks is performed to coincidence when OS can perform a multitask operation, this invention A waiting state arises at processing of synchronous data, and the technical problem that the case where it does not do at the transmission rate of the synchronous data which should be guaranteed arises is taken into consideration. Even when OS performs a multitask operation, it aims at offering the computer which can process synchronous data so that synchronous data can be transmitted at the transmission rate which should be guaranteed.

[0036] Moreover, this invention goes via the internal bus of the computer which two or more devices share from the IEEE1394 interface connected to one IEEE1394 bus. The technical problem that synchronous data cannot be sent to the IEEE1394 interface connected to another IEEE1394 bus is taken into consideration. It goes via the internal bus of the computer which two or more devices share from the IEEE1394 interface connected to one IEEE1394 bus. It aims at offering the computer which can send synchronous data to the IEEE1394 interface connected to another IEEE1394 bus.

[0037]

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the 1st this invention (it corresponds to claim 1) The synchronous device connected to the internal bus of the computer which two or more devices share, and said internal bus which transmits synchronous data to be guaranteed [of a transmission band] through said internal bus, The asynchronous device by which the guarantee of a transmission band was connected to said internal bus which transmits an unnecessary asynchronous data through said internal bus, As opposed to the use demand of said internal bus from

said synchronous device or said asynchronous device It is the computer characterized by having a bus mediation means to give priority to fairness or a synchronous device, and to give the licence of said bus, and CPU which controls processing or said synchronous device, and asynchronous device of the data transmitted through said internal bus means at least.
[0038] Moreover, the 2nd this invention (it corresponds to claim 2) is a computer given in the 1st this invention characterized by being PCI bus conformity physically [said internal bus] or logically.
[0039] The 3rd this invention (it corresponds to claim 3) moreover, said synchronous device which is connected to said internal bus and transmits data through said internal bus or said asynchronous device It has a timer means for guaranteeing the continuous duty time amount of said internal bus which can be written from the device connected to said internal bus physically or logically. Said bus mediation means By performing mediation which gives licence impartially to the use demand of said internal bus, and adjusting the preset value of said timer means by which said device connected to said internal bus physically or logically was built in each device It is a computer given in this invention of the 1st or 2 characterized by offering the transmission band guarantee of said synchronous data.
[0040] Moreover, the 4th this invention (it corresponds to claim 4) is a computer given in the 3rd this invention characterized by the mediation which gives licence to said fairness being mediation which gives licence with a round mold algorithm to said synchronization or said two or more internal bus use demands from an asynchronous device.
[0041] Moreover, the 5th this invention (it corresponds to claim 5) is a computer given in the 3rd this invention characterized by the mediation which gives licence to said fairness being mediation which gives the licence of the count of the same into predetermined time amount to said synchronization or said two or more internal bus use demands from an asynchronous device.
[0042] The 6th this invention (it corresponds to claim 6) moreover, adjustment of the preset value of said timer means Total of the preset values of said synchronous device which is connected to said internal bus and advances the use demand of said internal bus, and said all asynchronous devices is made into a denominator. The numeric value which used as the molecule the preset value of said synchronous device which uses said internal bus It is a computer given in either of the 3-5th this inventions characterized by the thing of the transmission rate which said synchronous device to the total rate of said internal bus which can be transmitted needs at least performed by [as becoming the above comparatively].
[0043] The 7th this invention (it corresponds to claim 7) moreover, said synchronous device which is connected to said internal bus and transmits data through said internal bus or said asynchronous device It has a timer means, in order to guarantee the continuous duty time amount of said internal bus which can be written from the device connected to said internal bus physically or logically. Said bus mediation means It is a computer given in this invention of the 1st or 2 characterized by performing mediation which gives licence with the priority to said synchronous device to the use demand of said internal bus, and offering the transmission band guarantee of said synchronous data.
[0044] Moreover, the 8th this invention (it corresponds to claim 8) is a computer given in the 7th this invention characterized by the mediation which gives the licence of said internal bus with the priority to said synchronous device being mediation which makes [more] the count of bus licence of said synchronous device than other devices.
[0045] The 9th this invention (it corresponds to claim 9) moreover, the count of licence of the bus of said synchronous device Total of said timer value of each device which is connected to said internal bus and advances the use demand of said internal bus, and the multiplication value of the count of bus licence of each device is made into a denominator. The numeric value which used as the molecule said timer value of said synchronous device which uses said internal bus, and the multiplication value of a bus use count It is a computer given in this invention of the 7th or 8 characterized by the thing of the transmission rate which said synchronous device to the total rate of said internal bus which can be transmitted needs at least performed by [as becoming the above comparatively].
[0046] Moreover, the 10th this invention (it corresponds to claim 10) is a computer given in either of the 1-9th this inventions characterized by said synchronous device being a transmission-line conversion

device which carries out the interface of the specific transmission line which can be transmitted synchronously and said specific internal bus.
[0047] Moreover, it is a computer given in the 10th this invention characterized by the transmission line which the 11th this invention (it corresponds to claim 11) can transmit [said / specific] synchronously being the bus of IEEE1394 specification conformity.
[0048] Moreover, the 12th this invention (it corresponds to claim 12) is a computer given in this invention of the 3rd characterized by the device connected to said internal bus physically or logically being said CPU, or ** 7.
[0049] Moreover, the 13th this invention (said synchronous device uses a predetermined value for claim 13 as its a preset value, correspondence transmits the value to said bus mediation means, and said bus mediation means is a computer given in the 7-9th this inventions characterized by carrying out priority mediation using the value.)
[0050] Moreover, the 14th this invention (it corresponds to claim 14) is a computer given in either of the 1-13th this inventions characterized by arbitrating said synchronous device as an asynchronous device, in case said synchronous device transmits an asynchronous data through said internal bus.
[0051] Moreover, the 15th this invention (it corresponds to claim 15) is a computer given in either of the 1-14th this inventions characterized by said CPU directing to said device that said device does not use said function, when the device connected to said internal bus has the function which uses a bus exceeding the time amount specified with said preset value.
[0052] Moreover, at least, the 16th this invention (it corresponds to claim 16) is equipped with memory, and the host bus of said CPU, said memory and the host bridge that transmits data mutually between said internal buses, and is a computer given in either of the 1-15th this inventions characterized by said host bridge guaranteeing synchronous data transmission in case said synchronous device connected to said internal bus transmits synchronous data to said memory.
[0053] Moreover, the 17th this invention (it corresponds to claim 17) is a computer given in either of the 1-16th this inventions characterized by having the host bridge which connects memory, the host bus of said CPU and said memory, and said internal bus, constituting said memory including the multiport memory which has at least two or more ports, and using at least 1 port for said synchronous data transmission only among said multiport.
[0054] Moreover, the 18th this invention (it corresponds to claim 18) is a computer given in the 17th this invention characterized by connecting the port of said dedication to the internal bus of said host bridge.
[0055] Moreover, the 19th this invention (it corresponds to claim 19) is a computer given in the 17th this invention characterized by connecting the port of said dedication to said internal bus.
[0056] Moreover, the 20th this invention (it corresponds to claim 20) It has the multitasking OS in which CPU, an IEEE1394 interface, and simultaneous processing of two or more tasks are possible. Said multitasking OS In case the task which carries out the real-time operation of the synchronous data transmitted to the synchronous data transmitted through said IEEE1394 interface or said IEEE1394 interface, and other tasks are performed to coincidence It is a computer given in the 11th this invention characterized by securing a CPU resource required for the task which carries out the real-time operation of said synchronous data at least, and guaranteeing said real-time operation.
[0057] Moreover, the 21st this invention (it corresponds to claim 21) is equipped with the internal bus of the computer to which two or more IEEE1394 interface and said two or more IEEE1394 interfaces are connected, and a original oscillation means to oscillate the HARASHIN number clock, and is a computer by which said two or more IEEE1394 interfaces are characterized by using the clock of 24.576MHz generated directly or indirectly or the integral multiple of those from said HARASHIN number clock.
[0058] Moreover, the 22nd this invention (it corresponds to claim 22) is a computer given in the 21st this invention characterized by being a PCI bus physically [said internal bus] or logically.
[0059] Moreover, the 23rd this invention (it corresponds to claim 23) is a computer given in this invention of the 21st or 22 characterized by the precision of said HARASHIN number clock being 100 ppm or less.

[0060] Moreover, it is a computer given in the 23rd this invention characterized by the precision of the clock of 24.576MHz generated from said HARASHIN number clock which uses the 24th this invention (it corresponds to claim 24) with said IEEE1394 interface, or the integral multiple of those being 100 ppm or less.
[0061] Moreover, the 25th this invention (it corresponds to claim 25) is a computer given in either of the 21-24th this inventions characterized by being directly transmitted to said two or more IEEE1394 interfaces, without having the 1st PLL means which generates the clock of 24.576MHz used with said two or more IEEE1394 interfaces from said HARASHIN number clock, or the integral multiple of those, and the clock of said 24.576MHz or integral multiple of those passing the signal line of said internal bus.
[0062] Moreover, it is a computer given in either of the 21-24th this inventions characterized by the 2nd PLL means and said two or more IEEE1394 interfaces to which the 26th this invention (it corresponds to claim 26) generates the clock of said internal bus from said HARASHIN number clock having the 3rd PLL means which generates the clock of 24.576MHz or the integral multiple of those from the clock of said internal bus.
[0063] Moreover, the 27th this invention (it corresponds to claim 27) is a computer given in the 26th this invention characterized by being n/m times [said 24.576MHz] (n and m being a positive integer) the frequency of the clock of said internal bus of this.
[0064] Moreover, the 28th this invention (it corresponds to claim 28) is a computer given in the 27th this invention to which n/m is characterized by **** which is 11/8, 3/2, or 5/4.
[0065] Moreover, the 29th this invention (it corresponds to claim 29) At least one IEEE1394 interface and said IEEE1394 interface, the cycle-time register of said IEEE1394 interface -- at least -- a bit pattern -- and It has the internal bus of the computer to which the cycle counter with the same frequency of the clock to count was connected. When said IEEE1394 interface becomes a cycle master, the value of said cycle counter is a computer characterized by being set to the cycle-time register within the IEEE1394 interface used as said cycle master.
[0066] Moreover, the 30th this invention (it corresponds to claim 30) is a computer given in the 29th this invention characterized by being PCI bus conformity physically [said internal bus] or logically.
[0067] Moreover, the 31st this invention (it corresponds to claim 31) the cycle-time register of an IEEE1394 interface -- at least -- a bit pattern -- and Two or more IEEE1394 interfaces which have the cycle counter to which the frequency of the clock to count is the same and minces the same time of day to each other, respectively, It has the internal bus of the computer to which said two or more IEEE1394 interfaces are connected. When said IEEE1394 interface becomes a cycle master, the IEEE1394 interface is a computer characterized by setting the value of one's cycle counter to one's cycle-time register.
[0068] Moreover, the 32nd this invention (it corresponds to claim 32) is a computer given in the 31st this invention characterized by being PCI bus conformity physically [said internal bus] or logically.
[0069] Moreover, the 33rd this invention (it corresponds to claim 33) is a computer given in the 32nd this invention by which it is characterized [to which the synchronization between said two or more cycle MUKAUNTA is carried out by coincidence reset at the time of power-on].
[0070] Moreover, the 34th this invention (it corresponds to claim 34) It has the internal bus of the computer to which two or more IEEE1394 interface and said two or more IEEE1394 interfaces were connected. From at least one source IEEE1394 interface in said two or more IEEE1394 interfaces The synchronous data which were transmitted to the internal bus of said computer and which contain a time stump at least When transmitting to an IEEE1394 bus through other destination IEEE1394 interfaces directly or indirectly, it is the computer characterized by having an operation means to add the time delay boiled and generated to said time stump by going via said internal bus at least.
[0071] Moreover, the 35th this invention (it corresponds to claim 35) The internal bus of said computer is an internal bus of multistage connection to which the internal bus with which plurality became independent was connected by the interior bus bridge of internal bus -. The IEEE1394 interface of said source and the IEEE1394 interface of the destination are respectively connected to said independent

internal bus. Said operation means by going via said interior bus bridge of internal bus - It is a computer given in the 34th this invention characterized by being with an operation means to add the time delay generated by going via the time delay to produce and each independent internal bus to said time stump.
[0072] Moreover, the 36th this invention (it corresponds to claim 36) is a program documentation medium characterized by recording the program for making either of the 1-35th this inventions perform the function of all or a part of means [all or a part of] of the computers of a publication by computer.
[0073]
[Embodiment of the Invention] Below, the gestalt of operation of this invention is explained with reference to a drawing.
[0074] (Gestalt of the 1st operation) The 1st configuration of the computer of the gestalt of operation is shown in drawing 1 . The gestalt of this operation explains the computer which can process synchronous data normally.
[0075] In drawing 1 , a computer consists of CPU1, the host bus 2, a host bridge 3, memory 5, graphics 6, a frame memory 7, PCI bus 8, disk I/F9, a device 10, and IEEE1394I/F 11-13.
[0076] Moreover, CD19 and HDD20 are connected to disk I/F9. The DTV tuner 24 is connected to IEEE1394I/F11 through the IEEE1394 bus 21. DVCR25 is connected to IEEE1394I/F12 through the IEEE1394 bus 22. HDD26 is connected to IEEE1394I/F13 through the IEEE1394 bus 23.
[0077] Moreover, a host bridge 3 has an arbiter 4. Moreover, disk I/F14, a device 10, and IEEE1394I/F 11-12 have the timer means 14-18, respectively.
[0078] CPUs1 are data processing and a means to perform an operation. The host bus 2 is a processor bus by which CPU1 and memory 5 are made as for data transmission to an epilogue and ultra high-speed. A host bridge 3 is a control chip which controls delivery of the data between CPU1, memory 5, and PCI bus 8. Memory 5 is SDRAM (synchronous dynamic access memory) which records data. Graphics 6 are means to be connected with a host bridge 3 by AGP which can carry out data transmission to a high speed, and to draw graphics at a high speed by it. A frame memory 7 is a means to hold the image data of a display screen as bit map data.
[0079] PCI bus 8 is a bus in the interior of the computer which two or more devices share. Disk I/F9 is an interface of SCSI conformity which connects CD19 and HDD20 with PCI bus 8. A device 10 is equipment connected to PCI bus 8. IEEE1394I/F 11-13 is the interface of the IEEE1394 conformity which ties PCI bus 8 and the IEEE1394 buses 21-23, respectively. The IEEE1394 buses 21-22 are buses of IEEE1394 conformity of another network which have the bus ID according to individual, respectively.
[0080] CD19 is equipment which reads the data of CD-ROM and is connected to disk I/F9. HDD20 is a hard disk which records data by random access or reads them, and is equipment connected to disk I/F9.
[0081] It connects with the IEEE1394 bus 21 and the DTV tuner 24 is a tuner which receives digital broadcast of CS broadcasting etc. It connects with the IEEE1394 bus 22 and DVCR25 is a digital video cassette recorder which performs record and playback of AV data. HDD26 is a hard disk which is connected to the IEEE1394 bus 22 and performs record and playback of AV data.
[0082] Moreover, IEEE1394 is the specification of an interface or a bus that real-time data to be guaranteed [of a transmission band] can be sent. The thing of the IEEE1394 interfaces 11-13 which can transmit synchronous data, and a call and synchronous data for the thing of such real-time data below is collectively called a synchronous device. Moreover, the thing of a device which transmits the data which do not need the guarantee of transmission bands, such as disk I/F9 and a device 10, is made to call an asynchronous data the thing of an asynchronous device and the data which do not need the guarantee of a call and a transmission band.
[0083] An arbiter 4 is a means to arbitrate any of a device (master device) which wish use of PCI bus 8 a bus royalty is granted.
[0084] The timer means 14-18 are means by which the maximum time amount which counts the time amount which is using PCI bus 8 per clock of PCI bus 8, and can use PCI bus 8 at once has the preset value described per clock of PCI bus 8.
[0085] Next, actuation of the gestalt of such this operation is explained.

[0086] With the gestalt of this operation, with the DTV tuner 24, CS broadcasting is received and the actuation in the case of recording received AV data by DVCR25 is explained.
[0087] AV data have been carried and sent to the broadcast wave from the broadcasting station of CS broadcasting using the transport packet of an MPEG 2 transport stream.
[0088] First, the DTV tuner 24 requires the transmission band for transmitting AV data to the device which is an isochronous resource manager among the equipment connected to the IEEE1394 bus 21. With the gestalt of this operation, since the equipment connected to the IEEE1394 bus 21 is two sets, IEEE1394I/F11 and the DTV tuner 24, either of these two sets of [inner] is an isochronous resource manager. An isochronous resource manager secures the transmission band for transmitting AV data according to the demand of the DTV tuner 24, and gives a channel number to the DTV tuner 24.
[0089] The DTV tuner 24 receives this broadcast wave, and gets over. And the DTV tuner 24 sends out AV data to which it restored to the IEEE1394 bus 21 as an isochronous packet one by one using the channel number to which it was given by the isochronous resource manager.
[0090] Time of day is divided into the time slot for 125 microseconds in IEEE1394. And 80% of time amount of the time amount of the 125 macro second of this time lot is used for an isochronous transfer, and the remaining 20% time amount is used for an asynchronous transfer. In an asynchronous transfer, the node ID of the equipment of the destination instead of a channel number is specified, and an asynchronous packet is transmitted. As an example of an asynchronous transfer, there are a command which controls equipment, a command for authentication between equipment, etc. However, with the gestalt of this operation, since its attention is paid about the case where synchronous data are transmitted, in order to make an understanding easy, description is omitted about an exchange of commands, such as control of a device and authentication.
[0091] The equipment connected to the IEEE1394 bus can send an isochronous packet only once by this time slot. That is, in IEEE1394, when transmitting data using an isochronous packet, each equipment transmits the data of a constant rate at a fixed period. And the amount of transmissions of the data which can be sent at a fixed period is guaranteed. Thus, in IEEE1394, synchronous data can be transmitted normally without lack.
[0092] IEEE1394I/F11 discriminates the isochronous packet which the DTV tuner 24 sent from a channel number, and receives. And received AV data are once stored in a buffer.
[0093] Furthermore, IEEE1394I/F11 requires a bus royalty of the arbiter 4 in a host bridge 3. An arbiter 4 performs a bus arbitration and grants a bus royalty to IEEE1394I/F11. Below, an arbiter 4 explains at a detail the actuation which performs a bus arbitration in this way.
[0094] Disk I/F9, a device 10, and IEEE1394I/F11 presuppose that it is the device (it is called a master device below) which wishes use of PCI bus 8. Disk I/F9, a disk 10, and IEEE1394I/F11 emit the demand of bus use to an arbiter 4. An arbiter 4 receives the demand of the bus use from such each master device. And while the demand of the bus use from two or more master devices is coming to coincidence, it is determined which master device a bus royalty is granted. And it notifies permitting use of PCI bus 8 to the master device which allows bus use. Between an arbiter 4 and each master device, it connects with the two signal lines REQ# and GNT#. REQ# and GNT# are point to point connections, and an arbiter 4 performs a bus arbitration using these two signal lines.
[0095] While receiving the demand of the bus use from two or more master devices to coincidence, an arbiter 4 arbitrates so that the count of authorization of bus use may become equal.
[0096] That is, as shown in (a) of drawing 2 , an arbiter 4 performs mediation which gives the authorization which uses PCI bus 8 according to a round mold algorithm.
[0097] In (a) of drawing 2 , three, an agent X27, an agent Y28, and an agent Z29, presuppose that there was an agent of PCI bus 8. If it does so, an arbiter 4 will presuppose that the licence of PCI bus 8 was first given to the agent X27. Next, an arbiter 4 gives an agent Y28 the licence of PCI bus 8. Furthermore, an arbiter 4 gives an agent Z29 the licence of PCI bus 8. Furthermore, an arbiter 4 gives an agent X27 the licence of PCI bus 8. In this way, an arbiter 4 gives the licence of PCI bus 8 so that each agent may be patrolled. Thus, the sequence that an arbiter 4 gives the licence of PCI bus 8 becomes as shown in (b) of drawing 2 . Since an arbiter 4 performs mediation which gives the authorization which

uses PCI bus 8 with the algorithm of such a round mold, disk I/F9, a device 10, and the count for which IEEE1394I/F11 uses PCI bus 8 become equal.
[0098] As a result of the bus arbitration by the arbiter 4, IEEE1394I/F11 obtained the licence of PCI bus 8, namely, presupposes that it was become the initiator of PCI bus 8. Then, the timer means 16 starts the count of the clock of PCI bus 8. And IEEE1394I/F11 can read AV data stored in the buffer one by one, can specify the address of IEEE1394I/F12, and can send out AV data to PCI bus 8 one by one until the counted value of the timer means 16 becomes equal to the preset value which the timer means 16 has beforehand. Namely, an initiator can perform data forwarding by making into the maximum time amount time amount to which the counted value of the timer means 16 becomes equal to a preset value. When AV data which should be sent out still remain temporarily and presetting time amount passes, bus use is stopped immediately and the licence of PCI bus 8 is again required of an arbiter 4.
[0099] Here, the preset value which the timer means 14-18 have needs to determine that the transmission rate which IEEE1394I/F11 needs will surely be securable. The decision approach of such a preset value is explained.
[0100] Suppose that the transmission rates which IEEE1394I/F11 should secure temporarily now are 100Mbps(es). And suppose that the maximum rate which can transmit PCI bus 8 is 1Gbps.
[0101] In such a case, since disk I/F9 transmitted a lot of data to PCI bus 8, a device 10 and disk I/F9 presuppose that the transmission rate which is transmitting data to PCI bus 8 reached for example, 950Mbps(es). If it does so, IEEE1394I/F11 can send AV data only at the transmission rate of 50Mbps (es). That is, from the DTV tuner 24, AV data will be sent at the transmission rate of 100Mbps(es), it will become the Bai grade of the transmission rate of AV data which IEEE1394I/F11 sends out, and the buffer of IEEE1394I/F11 will overflow immediately. It becomes impossible therefore, for IEEE1394I/F11 to carry out data transmission normally.
[0102] In order to avoid such a situation, the preset value of the timer means 14-18 is determined, and CPU1 is set up so that a required transmission rate can surely be secured, in case IEEE1394I/F11 sends out AV data to PCI bus 8.
[0103] That is, a preset value is decided that CPU1 fulfills several 1 conditions when the sum of two or more transmission rates which transmits PCI bus 8 exceeds the total transmission rate of PCI bus 8. Then, the transmission rate of IEEE1394I/F11 can be guaranteed.
[0104]
[Equation 1]

$$\frac{Rs}{Ra} \leq \frac{Ts}{\sum_{i=1}^{m} Ti}$$

Rs；伝送を希望する1つの同期デバイスが必要とする伝送レート

Ra；PCIバスの総伝送可能レート

Ts；伝送を希望する1つの同期デバイスのタイマー手段のプリセット値

$\sum_{i=1}^{m} Ti$；伝送を希望する同期デバイスと非同期デバイス全てのプリセット値の総和

[0105] Rs is a transmission rate which one synchronous device which wishes to transmit needs in several one. Moreover, Ra is the maximum rate which can transmit PCI bus 8. Moreover, TS is the preset value of a timer means of the above-mentioned synchronous device to wish to transmit. Ti is the preset value of the timer means of the specific synchronous device which wishes to transmit, or an asynchronous device.
[0106] That is, several one shows the following thing. or [namely, / that the rate of occupying to total of the preset value of the timer means of all synchronous devices which wish transmission of the preset value of the timer means of this synchronous device, and asynchronous devices is more nearly equal than the rate of occupying to the total rate of PCI bus 8 of the transmission rate which should be guaranteed for one synchronous device which wishes to transmit which can be transmitted] -- or it is made to become large
[0107] The transmission rate which IEEE1394I/F11 needs can be guaranteed by determining beforehand

the preset value of each timer means 14-18 so that such conditions may be fulfilled.
[0108] However, CPU1 shall be beforehand set up so that the command with which a master device disregards the preset value of a timer means, and performs data transmission may not be used. For example, Memory Write And It is made not to let it use the Invalidate command.
[0109] In addition, several 1 is required conditions when total of the transmission rate which each master device transmits becomes equal to the total rate of PCI bus 8 which can be transmitted, and total of the transmission rate which each master device transmits does not need to take several 1 conditions into consideration, when smaller than the total rate of PCI bus 8 which can be transmitted.
[0110] Moreover, timing to which CPU1 rewrites the preset value of each timer means 14-18 will be performed by the time either of IEEE1394I/F 11-13 sends out AV data to PCI bus 8. And the actuation whose either of IEEE1394I/F 11-13 sends out AV data to PCI bus 8 is good to start based on directions of CPU1, after CPU1 sets each preset value.
[0111] Now, IEEE1394I/F12 receives and once stores in a buffer AV data which did in this way and were sent out to PCI bus 8 from IEEE1394I/F11.
[0112] IEEE1394I/F12 requires the transmission band for transmitting AV data to the device which is an isochronous resource manager among the equipment connected to the IEEE1394 bus 22. With the gestalt of this operation, since the equipment connected to the IEEE1394 bus 22 is two sets, IEEE1394I/F12 and DVCR25, either of these two sets of [inner] is an isochronous resource manager. An isochronous resource manager secures the transmission band for transmitting AV data according to the demand of IEEE1394I/F12, and gives a channel number to IEEE1394I/F12.
[0113] IEEE1394I/F12 is sent out to the IEEE1394 bus 22 by making into an isochronous packet AV data stored in the buffer one by one using the channel number given by the isochronous resource manager.
[0114] DVCR25 discriminates the isochronous packet which IEEE1394I/F12 sent from a channel number, and receives. And received AV data are recorded on the tape medium one by one.
[0115] The broadcast wave received with the DTV tuner 24 as mentioned above is recorded on DVCR25.
[0116] Thus, when an arbiter 4 uses a round mold ARIGO rhythm, and it arbitrates so that the count of the authorization for which each device uses PCI bus 8 may become equal, and CPU1 adjusts the preset value of the timer means 14-18 of each device so that several 1 may be filled, IEEE1394I/F11 etc. can guarantee the amount of transmissions required for transmission of AV data.
[0117] In addition, with the gestalt of this operation, although it was explained having arbitrated the arbiter 4 so that the count of authorization might become equal using the algorithm of a round mold, it is not restricted to this. Mediation to which the count of the licence to each master device turns into a count of the same mostly by predetermined time amount to the use demand of PCI bus 8 from each master device not using a round mold algorithm is sufficient.

* NOTICES *

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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The synchronous device connected to the internal bus of the computer which two or more devices share, and said internal bus which transmits synchronous data to be guaranteed [of a transmission band] through said internal bus, The asynchronous device by which the guarantee of a transmission band was connected to said internal bus which transmits an unnecessary asynchronous data through said internal bus, As opposed to the use demand of said internal bus from said synchronous device or said asynchronous device The computer characterized by having a bus mediation means to give priority to fairness or a synchronous device, and to give the licence of said bus, and CPU which controls processing or said synchronous device, and asynchronous device of the data transmitted through said internal bus means at least.
[Claim 2] Said internal bus is a computer according to claim 1 characterized by being PCI bus conformity physically or logically.
[Claim 3] Said synchronous device which is connected to said internal bus and transmits data through said internal bus, or said asynchronous device It has a timer means for guaranteeing the continuous duty time amount of said internal bus which can be written from the device connected to said internal bus physically or logically. Said bus mediation means By performing mediation which gives licence impartially to the use demand of said internal bus, and adjusting the preset value of said timer means by which said device connected to said internal bus physically or logically was built in each device The computer according to claim 1 or 2 characterized by offering the transmission band guarantee of said synchronous data.
[Claim 4] The computer according to claim 3 characterized by the mediation which gives licence to said fairness being mediation which gives licence with a round mold algorithm to said synchronization or said two or more internal bus use demands from an asynchronous device.
[Claim 5] The computer according to claim 3 characterized by the mediation which gives licence to said fairness being mediation which gives the licence of the count of the same into predetermined time amount to said synchronization or said two or more internal bus use demands from an asynchronous device.
[Claim 6] Adjustment of the preset value of said timer means makes a denominator total of the preset values of said synchronous device which is connected to said internal bus and advances the use demand of said internal bus, and said all asynchronous devices. The numeric value which used as the molecule the preset value of said synchronous device which uses said internal bus The computer according to claim 3 to 5 characterized by the thing of the transmission rate which said synchronous device to the total rate of said internal bus which can be transmitted needs at least performed by [as becoming the above comparatively].
[Claim 7]

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CLAIMS

[Claim(s)]
[Claim 1] The synchronous device connected to the internal bus of the computer which two or more devices share, and said internal bus which transmits synchronous data to be guaranteed [of a transmission band] through said internal bus, The asynchronous device by which the guarantee of a transmission band was connected to said internal bus which transmits an unnecessary asynchronous data through said internal bus, As opposed to the use demand of said internal bus from said synchronous device or said asynchronous device The computer characterized by having a bus mediation means to give priority to fairness or a synchronous device, and to give the licence of said bus, and CPU which controls processing or said synchronous device, and asynchronous device of the data transmitted through said internal bus means at least.
[Claim 2] Said internal bus is a computer according to claim 1 characterized by being PCI bus conformity physically or logically.
[Claim 3] Said synchronous device which is connected to said internal bus and transmits data through said internal bus, or said asynchronous device It has a timer means for guaranteeing the continuous duty time amount of said internal bus which can be written from the device connected to said internal bus physically or logically. Said bus mediation means By performing mediation which gives licence impartially to the use demand of said internal bus, and adjusting the preset value of said timer means by which said device connected to said internal bus physically or logically was built in each device The computer according to claim 1 or 2 characterized by offering the transmission band guarantee of said synchronous data.
[Claim 4] The computer according to claim 3 characterized by the mediation which gives licence to said fairness being mediation which gives licence with a round mold algorithm to said synchronization or said two or more internal bus use demands from an asynchronous device.
[Claim 5] The computer according to claim 3 characterized by the mediation which gives licence to said fairness being mediation which gives the licence of the count of the same into predetermined time amount to said synchronization or said two or more internal bus use demands from an asynchronous device.
[Claim 6] Adjustment of the preset value of said timer means makes a denominator total of the preset values of said synchronous device which is connected to said internal bus and advances the use demand of said internal bus, and said all asynchronous devices. The numeric value which used as the molecule the preset value of said synchronous device which uses said internal bus The computer according to claim 3 to 5 characterized by the thing of the transmission rate which said synchronous device to the total rate of said internal bus which can be transmitted needs at least performed by [as becoming the above comparatively].
[Claim 7] Said synchronous device which is connected to said internal bus and transmits data through said internal bus, or said asynchronous device It has a timer means, in order to guarantee the continuous duty time amount of said internal bus which can be written from the device connected to said internal bus physically or logically. Said bus mediation means The computer according to claim 1 or 2

characterized by performing mediation which gives licence with the priority to said synchronous device to the use demand of said internal bus, and offering the transmission band guarantee of said synchronous data.
[Claim 8] The computer according to claim 7 characterized by the mediation which gives the licence of said internal bus with the priority to said synchronous device being mediation which makes [more] the count of bus licence of said synchronous device than other devices.
[Claim 9] The count of licence of the bus of said synchronous device makes a denominator total of said timer value of each device which is connected to said internal bus and advances the use demand of said internal bus, and the multiplication value of the count of bus licence of each device. The numeric value which used as the molecule said timer value of said synchronous device which uses said internal bus, and the multiplication value of a bus use count The computer according to claim 7 or 8 characterized by the thing of the transmission rate which said synchronous device to the total rate of said internal bus which can be transmitted needs at least performed by [as becoming the above comparatively].
[Claim 10] Said synchronous device is a computer according to claim 1 to 9 characterized by being the transmission-line conversion device which carries out the interface of the specific transmission line which can be transmitted synchronously and said specific internal bus.
[Claim 11] The computer according to claim 10 characterized by the transmission line in which said specific synchronous transmission is possible being the bus of IEEE1394 specification conformity.
[Claim 12] A computer given in claim 3 or ******** 7 characterized by the device connected to said internal bus physically or logically being said CPU.
[Claim 13] It is the computer according to claim 7 to 9 which said synchronous device transmits the value to said bus mediation means using a predetermined value as its a preset value, and is characterized by said bus mediation means carrying out priority mediation using the value.
[Claim 14] It is the computer according to claim 1 to 13 characterized by arbitrating said synchronous device as an asynchronous device in case said synchronous device transmits an asynchronous data through said internal bus.
[Claim 15] Said CPU is a computer according to claim 1 to 14 characterized by directing to said device that said device does not use said function when the device connected to said internal bus has the function which uses a bus exceeding the time amount specified with said preset value.
[Claim 16] It is the computer according to claim 1 to 15 which is equipped with memory and the host bridge which transmits data mutually between the host bus of said CPU, said memory, and said internal bus at least, and is characterized by said host bridge guaranteeing synchronous data transmission in case said synchronous device connected to said internal bus transmits synchronous data to said memory.
[Claim 17] It is the computer according to claim 1 to 16 characterized by having the host bridge which connects memory, the host bus of said CPU and said memory, and said internal bus, constituting said memory including the multiport memory which has at least two or more ports, and using at least 1 port for said synchronous data transmission only among said multiport.
[Claim 18] The port of said dedication is a computer according to claim 17 characterized by connecting with the internal bus of said host bridge.
[Claim 19] The port of said dedication is a computer according to claim 17 characterized by connecting with said internal bus.
[Claim 20]